



## **Technical Specification**

for

### **Digital Interfaces based on hierarchical bit rates of 2048 kbit/s, 34 368 kbit/s and 139 264 kbit/s**

#### **IDA TS DLCN**

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**NOTICE**

**This Specification is subject to review and revision.**

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## Part A Introduction

### 1 Scope

- 1.1** Part B of this Specification defines the physical and electrical characteristics of interfaces at hierarchical bit rates of 2048 kbit/s, 34 368 kbit/s and 139 264 kbit/s. For signals with bit rates of  $n \times 64$  kbit/s ( $n = 2$  to 31), which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface.
- 1.2** Part C defines the functional characteristics of 2048 kbit/s interface associated with synchronous digital multiplex equipment and digital exchanges in IDN for telephony and ISDN and PCM multiplexing equipment. It defines the basic frame structure at 2048 kbit/s, including details of frame length, frame alignment signal, cyclic redundancy check procedures and other basic information. It also defines specific information about how certain channels at 64 kbit/s and other bit rates are accommodated within the basic frame structure at 2048 kbit/s.
- 1.3** Part D is relevant to equipment that receives signals with basic frame structure at 2048 kbit/s as described in Part C. It defines the frame alignment and CRC procedure to be used by such equipment
- 1.4** Part E provides the mappings to be used for the transport of ATM cells over PDH at hierarchical bit rates of 2048 kbit/s, 34 368 kbit/s and 139 264 kbit/s.

### 2 General Requirements

#### 2.1 Power Supply

The equipment may be a.c. powered or d.c. powered. For an a.c. powered equipment, the Specification shall be complied with when operating from an a.c. mains supply of voltage,  $230V \pm 10\%$  and frequency,  $50 \text{ Hz} \pm 2\%$ . Where external power supply is used, e.g. AC adaptor, it shall not affect the capability of the equipment to meet the Specification.

#### 2.2 Identification of Equipment

The equipment shall be marked with the supplier or manufacturer's name or identification mark, and the supplier or manufacturer's model or type reference. The markings required shall be legible, indelible and readily visible.

### 3 Electromagnetic Compatibility & Electrical Safety Requirements

- 3.1** The equipment shall comply with the limits for conducted disturbance at the mains terminals and telecommunication ports, and the limits for radiated disturbance defined in the IEC CISPR 22.
- 3.2** The equipment shall comply with the IEC 60950-1 safety standard<sup>1</sup>. The requirements in IEC 60950-1 that are applicable to the equipment [e.g. class of equipment, type of telecommunication network voltage (TNV) circuit and types of components] shall be identified and complied with.

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<sup>1</sup> The safety standard includes, among others, protection of telecommunications network service personnel and users of other equipment connected to the network from hazards in the equipment.

Note:

The following notations are used in the Specification:

- CR Conformance requirement defines features and functions which must be supported at minimum.
- M Mandatory requirements
- O Optional requirements
- NA Not Applicable
- GID General Information and Definitions

## Part B Physical/Electrical characteristics of hierarchical digital interfaces based on the first level bit rate of 2048 kbit/s

(Sections 4 and 9 to 13, ITU-T Recommendation G.703, 11/2001)

Title	ITU-T Rec. G.703	CR	Remarks
<b>Interface at 64 kbit/s (E0)</b>	<b>4</b>	–	Heading
<b>Functional requirement</b> – 64 kbit/s information signal – 64 kHz timing signal – 8 kHz timing signal	<b>4.1</b>	M Note 1	In both directions of transmission, three signals can be carried across the interface.
Three types of envisaged interfaces	4.1.1	–	Heading
Co-directional interface	4.1.1.1	M Note 2	
Centralised clock interface	4.1.1.2	NA	
Contra-directional interface	4.1.1.3	NA	
<b>Electrical characteristics</b>	<b>4.2</b>	–	
Electrical characteristics of 64 kbit/s co-directional interface	4.2.1	–	Heading
General	4.2.1.1	M	
Specifications at the output ports (Table 1/G.703)	4.2.1.2	M Note 3	
Specifications at the input ports	4.2.1.3	M	
Grounding of screen	4.2.1.4	M	
Electrical characteristics of 64 kbit/s centralised clock interface	4.2.2	NA	
Electrical characteristics of 64 kbit/s contra-directional interface	4.2.3	NA	
<b>Interface at 2048 kbit/s</b>	<b>9</b>	–	Heading
<b>General characteristics</b>	<b>9.1</b>	Note 4	
<b>Specifications at the output ports</b>	<b>9.2</b>	Note 4	
<b>Specifications at the input ports</b>	<b>9.3</b>	Note 4	
<b>Grounding of outer conductor or screen</b>	<b>9.4</b>	Note 4	
<b>Interface at 8448 kbit/s</b>	<b>10</b>	NA	
<b>Interface at 34 368 kbit/s</b>	<b>11</b>	–	Heading
<b>General characteristics</b>	<b>11.1</b>	Note 5	
<b>Specifications at the output ports</b>	<b>11.2</b>	Note 5	
<b>Specifications at the input ports</b>	<b>11.3</b>	Note 5	
<b>Grounding of outer conductor</b>	<b>11.4</b>	Note 5	
<b>Interface at 139 264 kbit/s</b>	<b>12</b>	–	Heading
<b>General characteristics</b>	<b>12.1</b>	Note 6	
<b>Specifications at the output ports</b>	<b>12.2</b>	Note 6	
<b>Specifications at the input ports</b>	<b>12.3</b>	Note 6	
<b>Grounding of outer conductor</b>	<b>12.4</b>	Note 6	

Title	ITU-T Rec. G.703	CR	Remarks
<b>2048 kbit/s synchronisation interface</b>	<b>13</b>	–	Heading
<b>General</b>	<b>13.1</b>	Note 7	
<b>Specifications at the output ports</b>	<b>13.2</b>	Note 7	
<b>Specifications at the input ports</b>	<b>13.3</b>	Note 7	
<b>Grounding of outer conductor or screen</b>	<b>13.4</b>	Note 7	
<b>Definition of codes</b>	<b>Annex A</b>	GID	
<p>Note 1 – The 64 kbit/s information and the 64 kHz timing signals are mandatory. Although the controlling equipment must generate the 8kHz timing (e.g. PCM multiplex or time slot access equipment), it is not mandatory for the subordinate equipment to utilise the 8 kHz timing signal or to supply an 8 kHz timing signal.</p> <p>Note 2 – The equipment shall synchronise its bit timing to the signal received from the network. In the event of loss of received signal the equipment shall derive its output timing from its internal clock.</p> <p>Note 3 – Specifications are valid for equipment of the 2 Mbit/s hierarchy.</p> <p>Note 4 – Requirements are mandatory for Digital Interface at 2048 kbit/s. They are also applicable to the Physical Medium Dependent (PMD) sublayer of the ATM Forum E1 Physical Layer Interface (af-phy-0064.000, section 3).</p> <p>Note 5 – Requirements are mandatory for Digital Interface at 34 368 kbit/s. They are also applicable to the Physical Medium Dependent (PMD) sublayer of ATM Forum E3 Physical Layer Interface (af-phy-0034.000, section 2.5.3).</p> <p>Note 6 – Requirements are mandatory for Digital Interface at 139 264 kbit/s.</p> <p>Note 7 – Requirements are mandatory if digital equipment synchronises with an external 2048 kHz synchronisation signal.</p>			

## Part C Synchronous frame structures used at 2048 kbit/s hierarchical level

(Sections 2.3 and 5, ITU-T Recommendation G.704, 10/1998)

Title	ITU-T Rec. G.704	CR	Remarks
<b>Basic frame structure at 2048 kbit/s</b>	<b>2.3</b>	–	Heading
Frame length	2.3.1	Note 1	
Allocation of bits number 1 to 8 of the frame	2.3.2	Note 1	
Description of the CRC-4 procedure in bit 1 of the frame	2.3.3	Note 1	
Synchronisation status: $S_{an}$	2.3.4	Note 1	
<b>Characteristics of frame structures carrying channels at various bit rates in 2048 kbit/s interface</b>	<b>5</b>	–	Heading
<b>Interface at 2048 kbit/s carrying 64 kbit/s channels</b>	<b>5.1</b>	–	Heading
Frame structure	5.1.1	–	Heading
Number of bits per 64 kbit/s channel time slot	5.1.1.1	Note 2	
Number of 64 kbit/s channel time slots per frame	5.1.1.2	Note 2	
Allocation of the bits of 64 kbit/s channel time slot 0	5.1.1.3	Note 2	
Use of other 64 kbit/s channel time slot 0	5.1.2	Note 2	
Signalling	5.1.3	Note 2	
<b>Interface at 2048 kbit/s carrying n x 64 kbit/s</b>	<b>5.2</b>	Note 2	
One n x 64 kbit/s signal on the tributary side of a multiplex equipment	5.2.1	Note 2	
One n x 64 kbit/s signal on the multiplexed signal side of a multiplexing equipment	5.2.2	Note 2	
<p>Note 1 – Requirements are mandatory for frame structure at 2048 kbit/s. They are also applicable to the Transport Specific TC (Transmission Convergence sublayer) Functions of ATM Forum E1 Physical Layer Interface (af-phy-0064.000, section 4.1).</p> <p>Note 2 – Requirements are mandatory for frame structure carrying channels at various bit rates in 2048 kbit/s interface. They are also applicable to the Transport Specific TC (Transmission Convergence sublayer) Functions of ATM Forum E1 Physical Layer Interface (af-phy-0064.000, section 4.1).</p>			

**Part D Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structure at 2048 kbit/s**  
(Section 4, ITU-T Recommendation G.706, 04/1991)

Title	ITU-T Rec. G.706	CR	Remarks
<b>Frame alignment and CRC procedures at 2048 kbit/s interface</b>	<b>4</b>	–	Heading
<b>Loss and recovery of frame alignment</b>	<b>4.1</b>	–	Heading
Loss of frame alignment	4.1.1	Note 1	
Strategy for frame alignment recovery	4.1.2	Note 1	
<b>CRC multiframe alignment using information in bit 1 of the basic frame</b>	<b>4.2</b>	Note 1	
<b>CRC bit monitoring</b>	<b>4.3</b>	Note 1	
Monitoring procedure	4.3.1	Note 1	
Monitoring for false frame alignment	4.3.2	Note 1	
Error performance monitoring using CRC-4	4.3.3	Note 1	
Background information on the use of CRC procedures	Annex A	GID	
Modified CRC multiframe alignment algorithm to allow automatic interworking between equipment with and without CRC-4 capability	Annex B	Note 1	
CRC-4 checksum updating procedure at intermediate path points in a message-based data-link application	Annex C	Note 1	
Note 1 – Requirements are mandatory for frame structure at 2048 kbit/s. They are also applicable to the Transport Specific TC (Transmission Convergence sublayer) Functions of ATM Forum E1 Physical Layer Interface (af-phy-0064.000, section 4.1).			

## Part E ATM cells mapping into 2048 kbit/s, 34 368 kbit/s and 139 264 kbit/s

(Sections 3, 6 and 9, ITU-T Recommendation G.804, 06/2004)

Title	ITU-T Rec. G.804	CR	Remarks
<b>Mapping of ATM cells into 2048 kbit/s</b>	<b>3</b>	–	Heading
<b>Frame format</b>	<b>3.1</b>	Note 1	Note 2
<b>Cell rate adaptation</b>	<b>3.2</b>	Note 1	I.432.1, clause 4.3.5
<b>Header error control (HEC) generation</b>	<b>3.3</b>	Note 1	I.432.1, clause 4.3.2
<b>Scrambling of the ATM cell payload</b>	<b>3.4</b>	Note 1	I.432.1, clause 4.3.4
<b>Cell delineation</b>	<b>3.5</b>	Note 1	I.432.1, clause 4.3.3
<b>Cell header verification and extraction</b>	<b>3.6</b>	Note 1	I.432.1, clause 4.3.3
<b>Physical layer OAM</b>	<b>3.7</b>	Note 1	Note 3
<p>Note 1 – Requirements are mandatory for transporting ATM cells over PDH (Plesiochronous Digital Hierarchy) network at 2048 kbit/s. They are also applicable to the ATM-Specific TC (Transmission Convergence sublayer) Functions of ATM Forum E1 Physical Layer Interface (af-phy-0064.000, section 4.2).</p> <p>Note 2 – The basic frame structure at 2048 kbit/s is as described in Part C and Part D of this Specification. The ATM cell is mapped into bits 9 to 128 and bits 137 to 256 (i.e. time slots 1 to 15 and time slots 17 to 31 of the 2048 kbit/s frame with octet structure of cell aligned with the octet structure of the frame (Figure 3-1/G.804)</p> <p>Note 3 – Overhead bits for physical layer OAM functionality are defined in Part D of this Specification.</p>			

Title	ITU-T Rec. G.804	CR	Remarks
<b>Mapping of ATM cells into 34 368 kbit/s</b>	<b>6</b>	–	Heading
<b>Frame format</b>	<b>6.1</b>	Note 1	Note 2
<b>Cell rate adaptation</b>	<b>6.2</b>	Note 1	I.432.1, clause 4.3.5
<b>Header error control (HEC) generation</b>	<b>6.3</b>	Note 1	I.432.1, clause 4.3.2
<b>Scrambling of the ATM cell payload</b>	<b>6.4</b>	Note 1	I.432.1, clause 4.3.4
<b>Cell delineation</b>	<b>6.5</b>	Note 1	I.432.1, clause 4.3.3
<b>Cell header verification and extraction</b>	<b>6.6</b>	Note 1	I.432.1, clause 4.3.3
<b>Physical layer OAM</b>	<b>6.7</b>	Note 1	Note 3
<p>Note 1 – Requirements are mandatory for transporting ATM cells over PDH network at 34 368 kbit/s. They are also applicable to the Transport-Specific and ATM-Specific TC (Transmission Convergence sublayer) Functions of ATM Forum E3 Physical Layer Interface (af-phy-0034.000, section 2.5.4).</p> <p>Note 2 – The basic frame structure at 34 368 kbit/s is as described in ITU-T Rec. G.832, clause 2.1. The ATM cells are mapped into the 530 payload octets of the 34 368 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (Figure 6-1/G.804).</p> <p>Note 3 – Overhead bits for physical layer OAM functionality are defined in ITU-T Rec. G.832, clause 2.1.2.</p>			

Title	ITU-T Rec. G.804	CR	Remarks
<b>Mapping of ATM cells into 139 264 kbit/s</b>	<b>9</b>		
<b>Frame format</b>	<b>9.1</b>	Note 1	Note 2
<b>Cell rate adaptation</b>	<b>9.2</b>	Note 1	I.432.1, clause 4.3.5
<b>Header error control (HEC) generation</b>	<b>9.3</b>	Note 1	I.432.1, clause 4.3.2
<b>Scrambling of the ATM cell payload</b>	<b>9.4</b>	Note 1	I.432.1, clause 4.3.4
<b>Cell delineation</b>	<b>9.5</b>	Note 1	I.432.1, clause 4.3.3
<b>Cell header verification and extraction</b>	<b>9.6</b>	Note 1	I.432.1, clause 4.3.3
<b>Physical layer OAM</b>	<b>9.7</b>	Note 1	Note 3
<p>Note 1 – Requirements are mandatory for transporting ATM cells over PDH network at 139 264 kbit/s.</p> <p>Note 2 – The basic frame structure at 139 264 kbit/s is as described in ITU-T Rec. G.832, clause 2.4. The ATM cells are mapped into the 2160 payload octets of the 139 264 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (Figure 9-1/G.804)</p> <p>Note 3 – Overhead bits for physical layer OAM functionality are defined in ITU-T Rec.G.832, clause 2.4.2.</p>			

## Annex A: References

For the technical requirements captured in this Specification, reference has been made to the following documents:

ITU-T Rec. G.703 (11/2001)	Physical / electrical characteristics of hierarchical digital interfaces
ITU-T Rec. G.704 (10/1998)	Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels
ITU-T Rec. G.706 (04/1991)	Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704
ITU-T Rec. G.804 (06/2004)	ATM cell mapping into plesiochronous digital hierarchy (PDH)
ITU-T Rec. G.823 (1993)	The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
ITU-T Rec. G.832 (1998)	Transport of SDH elements on PDH networks – Frame and multiplexing
ITU-T Rec. I.432.1 (02/1999)	B-ISDN user-network interface – Physical layer specification: General characteristics
ITU-T Rec. K.41 (1998)	Resistibility of internal interfaces of telecommunication centres to surge overvoltages
IEC 60950-1: 2001	Information Technology Equipment – Safety
IEC CISPR 22: 2003-04	Information Technology Equipment – Radio disturbance characteristics – Limits and methods of measurement
ETS 300 166 (August 1993)	Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s – based plesiochronous or synchronous digital hierarchies
ETS 300 167 (August 1993)	Functional characteristics of 2048 kbit/s interfaces
ETS 300 337 (February 1995)	Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical bit rates of 2048 kbit/s, 34 368 kbit/s and 139 264 kbit/s
Af-phy-0064.000 (September 1996)	The ATM Forum Technical Committee – E1 Physical Interface Specification
Af-phy-00.364.000 (August 1995)	The ATM Forum Technical Committee – E3 Public UNI

## Annex B: Addendum/Corrigendum

Changes to IDA TS DLCN 1 Issue 2			
Page	TS Ref.	Items Changed	Effective Date
—	—	<p>The IDA Technical Specification (IDA TS DLCN Issue 1) has superseded the IDA Type Approval Specification for Digital Interfaces based on hierarchical bit rates of 2048 kbit/s, 34,368 kbit/s and 139,264 kbit/s (IDA TS DLCN 1 Issue 2).</p> <p>The Technical Specification has also incorporated the EMC requirements, previously published under the IDA TS EMC Issue 1 Rev 1.</p> <p>Changes are mainly editorial in nature, in which the essential technical requirements for compliance remain unchanged.</p>	21 Jul 05